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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/667,164	09/21/2000	William E. Ballachino	00-C-050 (STMI01-00050	8138

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EXAMINER
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ART UNIT	PAPER NUMBER
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/667,164	BALLACHINO, WILLIAM E.	
	Examiner	Art Unit	
	CHAT C. DO	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,8-16 and 19-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-16 and 19-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 12/28/2007.

2. Claims 1-5, 8-16, and 19-31 are pending in this application. Claims 1, 12, and 23 are independent claims. In Amendment, claims 6-7 and 17-18 are previously cancelled. This Office Action is made final.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1-5, 8-16, and 19-31 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-5, 8-16, and 19-31 cite an adder for adding two arguments in accordance with a mathematical algorithm. However, claims 1-5, 8-16, and 19-31 merely disclose series mental steps/components for adding two arguments without disclosing a practical/physical application. Further, the claims appear to preempt every substantial practical application of the idea embodied by the claim. Therefore, claims 1-5, 8-16, and 19-31 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5, 8-16, and 19-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Uya (U.S. 4,682,303).

Re claim 1, Uya discloses in Figure 2 an M-bit adder (e.g. an adder in Figure 2 wherein M is equate to 26) capable of receiving a first M-bit argument (e.g. first argument as A0-A25), a second M-bit argument (e.g. second argument as B0-B25), and a carry-in "Ci" (e.g. C4, C8, C13, C19, and C26 into respective cells) bit comprising:

M adder cells arranged in R rows (e.g. as seen in Figure 2 wherein the cell for adding bits 13-18 includes components 34-35, 40-41, and 43), wherein a least significant adder cell in a first one of rows of adder cells (e.g. the first adder of every set of adder) is operable to:

receive a first data bit, Ax, from first M-bit argument and a first data bit, Bx, from second M-bit argument (e.g. A_4 and B_4 respectively in Figure 2),

generate a first conditional carry-out bit, Cx(1) (e.g. C_8^1 from 21 in Figure 2 in P2 cell), and a second conditional carry-out bit, Cx(0) (e.g. C_8^0 from 20 in Figure 2 in P2 cell), and

provide the first and second conditional carry-out bits (e.g. output of C_8^1 and C_8^0 in Figure 2) to another of adder cells (e.g. the outputs of carry are fed to logic gates 24 and 25 of next cell P3),

wherein $C_x(1)$ bit is calculated assuming a row carry-out bit from a second row of adder cells preceding first row is a 1 (e.g. expression 2 in col. 3) and Cx(0) bit is

calculated assuming row carry-out bit from second row is a 0 (e.g. expression 4 in col. 4); and

wherein the second one of the adder cells (e.g. the second cell is the cell receives the carry-out bits from the previous first cell) in the first one of the rows is operable to:

receive a first data bit, A_{x+1} from the first M-bit argument and a first data bit, B_{x+1}, from the second M-bit argument (e.g. Figures 3-4 wherein each block of computation can be done/performed for only a single input bit of operand),

receive both the first conditional carry-out bit, $C_x(1)$ and the second conditional carry-out bit, $C_x(0)$ (e.g. both C_{19}^1 as conditional carry-out bit Cx^1 and C_{19}^0 as conditional carry-out bit C_x^0 are inputted into the logic circuit XOR-NNAND of the next cell as seen in Figure 2);

generate both a first conditional carry-out bit, $C_{x+1}(1)$, and a second conditional carry-out bit, $C_{x+1}(0)$ (e.g. C_{25}^1 and C_{25}^0 respectively in Figure 2) by propagating the first conditional carry-out bit, $C_x(1)$ and the second conditional carry-out bit, $C_x(0)$ through a first pass gate and a second pass gate (e.g. logic gates 54-55 in Figure 2), respectively, when the first data bit A_{x+1} and the second data bit B_{x+1} are not equal (e.g. as high or low logic for the logic 54 in Figure 2), and

output the first and second conditional carry-out bit $C_{x+1}(1)$ and $C_{x+1}(0)$ to other circuitry (e.g. C_{25}^1 and C_{25}^0 respectively in Figure 2 for the next bit set).

Re claim 2, Uya further discloses in Figure 2 least significant adder cell generates a first conditional sum bit (e.g. $S^0$4 in Figure 2), and a second conditional sum bit (e.g. $S^1$4 in Figure 2).

Re claim 3, Uya further discloses in Figure 2 Sx(1) bit is calculated assuming row carry-out bit from second row is a 1 (e.g. 65) and Sx(0) bit is calculated assuming 4 row carry-out bit from second row is a 0 (e.g. 70).

Re claim 4, Uya further discloses in Figure 2 row carry-out bit selects one of Sx(1) bit and Sx(0) bit to be output by least significant adder cell (e.g. 32).

Re claim 5, Uya further discloses in Figure 2 other circuitry comprises: a third adder cell in the first one of rows of adder cells, and wherein the third adder cell receives a third data bit, A_{x+2}, from the first M-bit argument and a third data bit, $B_{x+2,}$ from the second M-bit argument, and receives from the second adder cell $C_{x+1}(1)$ bit and the $C_{x+1}(0)$ bit (e.g. repeat the process as seen in Figure 2 and claim 1 for the next cell in the row).

Re claim 8, Uya further discloses in Figures 1-4 second adder cell (e.g. adder for adding A5 and B5) generates a first conditional sum bit S1 (e.g. S5 in Figure 3), wherein S1 bit is generated from A5 data bit, B5 data bit, and CH0 bit from least significant adder cell.

Re claim 9, Uya further discloses in Figures 1-4 second adder cell (e.g. adder for adding A5 and B5) generates a second conditional sum bit, wherein S1 (e.g. S5 in Figure 4) bit is generated from A5 data bit, B5 data bit, and CL0 bit from least significant adder cell.

Re claim 10, Uya further discloses in Figures 1-4 row carry-out bit selects one of Sl(1) bit and Sl(0) bit to be output by second adder cell (e.g. 24 and 25 in Figure 2).

Re claim 11, Uya further discloses first row of adder cells contains N adder cells and second row of adder cells preceding first row contains less than N adder cells (e.g. P3, P4, and P5 wherein P3 has 5 adder cells, P4 has 6 adder cells, and P5 has 5 adder cells).

Re claim 12, it is a processor claim of claim 1. Thus, claim 12 is also rejected under the same rationale in the rejection of rejected claim 1.

Re claim 13, it is a processor claim of claim 2. Thus, claim 13 is also rejected under the same rationale in the rejection of rejected claim 2.

Re claim 14, it is a processor claim of claim 3. Thus, claim 14 is also rejected under the same rationale in the rejection of rejected claim 3.

Re claim 15, it is a processor claim of claim 4. Thus, claim 15 is also rejected under the same rationale in the rejection of rejected claim 4.

Re claim 16, it is a processor claim of claim 5. Thus, claim 16 is also rejected under the same rationale in the rejection of rejected claim 5.

Re claim 17, it is a processor claim of claim 6. Thus, claim 17 is also rejected under the same rationale in the rejection of rejected claim 6.

Re claim 18, it is a processor claim of claim 7. Thus, claim 18 is also rejected under the same rationale in the rejection of rejected claim 7.

Re claim 19, it is a processor claim of claim 8. Thus, claim 19 is also rejected under the same rationale in the rejection of rejected claim 8.

Re claim 20, it is a processor claim of claim 9. Thus, claim 20 is also rejected under the same rationale in the rejection of rejected claim 9.

Re claim 21, it is a processor claim of claim 10. Thus, claim 21 is also rejected under the same rationale in the rejection of rejected claim 10.

Re claim 22, it is a processor claim of claim 11. Thus, claim 22 is also rejected under the same rationale in the rejection of rejected claim 11.

Re claim 23, it is a method claim of claim 1. Thus, claim 23 is also rejected under the same rationale in the rejection of rejected claim 1.

Re claim 24, Uya further discloses in Figure 2 the second adder cell further comprises: a first inverter operable for inverting said first conditional carry-out bit Cx(1) transmitted through said first pass gate prior to outputting said first conditional carry-out bit Cv(1) (e.g. AND and INVERT logic as seen in Figure 3 prior outputting C_8^1); and a second inverter operable for inverting said second conditional carry-out bit Cv(0) transmitted through said second pass gate prior to outputting said second conditional carry-out bit Cv(0) (e.g. AND and INVERT logic as seen in Figure 3 prior outputting C_8^0).

Re claim 25, Uya further discloses in Figure 2 second adder cell further comprises: a first inverter operable for inverting said received conditional carry-out bit Cx(1) prior to transmission through said first pass gate (e.g. AND and INVERT logic as seen in Figure 3 prior outputting C_8^1 to transmitted to the NAND gate 24 in Figure 2); and a second inverter operable for inverting said received second conditional carry-out bit Cx(0) prior to transmission through said second pass gate (e.g. AND and INVERT logic as seen in Figure 3 prior outputting C_8^0 to transmitted to the OR gate 24 in Figure 2).

Re claim 26, Uya further discloses in Figure 2 other circuitry comprises: a row multiplexer, wherein said row carry-out bit from said second row of adder cells preceding said first row selects one of said Cx+l(1) bit and said Cx+l(0) bit to be output by said row multiplexer (e.g. multiplexer 43 in Figure 2).

Re claim 27, Uya further discloses in Figure 2 first adder cell comprises: a first multiplexer operable for receiving said first conditional sum bit, Sx(1) and said second conditional sum bit Sx(0), wherein said row carry-out bit selects one of said Sx(1) bit and said Sx(0) bit to be output by said first adder cell (e.g. multiplexer 33 in Figure 2); and said second adder cell comprises: a second multiplexer operable for receiving said second conditional sum bit Sx+ i(1) and said second conditional sum bit Sx+ j(0), wherein said row carry-out bit selects one of said Sx+ I(1) bit and said Sx+~(0) bit to be output by said second adder cell (e.g. multiplexer 43 in Figure 2).

Re claim 28, it is a processor claim of claim 24. Thus, claim 28 is also rejected under the same rationale in the rejection of rejected claim 24.

Re claim 29, it is a processor claim of claim 25. Thus, claim 29 is also rejected under the same rationale in the rejection of rejected claim 25.

Re claim 30, it is a processor claim of claim 26. Thus, claim 31 is also rejected under the same rationale in the rejection of rejected claim 26.

Re claim 31, it is a processor claim of claim 27. Thus, claim 31 is also rejected under the same rationale in the rejection of rejected claim 27.

Response to Arguments

7. Applicant's arguments filed 12/28/2007 have been fully considered but they are not persuasive.

a. The applicant argues in pages 16-17 for claims rejected under 35 U.S.C. 101 that the claims are directed to statutory subject matter since the apparatus clearly defines structure operable for performing various functions wherein the functions include generating conditional carry-out bits and propagating through pass gates and outputting two conditional carryout bits to other circuitry.

The examiner respectfully submits that the claims, particularly claim 23, are just merely abstract idea or disclosing series of mental steps for performing intended function which is to add two operands together. As clearly stated in the above rejection, the claims lack of practical applications and are preempt substantial applications. These two issues cannot overcome with propagating through pass gates and outputting conditional carry-out bits to other circuitry wherein passing gate can be a logical step.

b. The applicant argues in page 18 first paragraph for claims rejected under 35 U.S.C. 102(b) that the cited reference fails to disclose the claimed invention because first, Bit 0 adder cell does not receive any conditional carryout bits, the Bit 0 adder cannot meet this limitation; and second, the conditional carryout bits generated by the LSB adder of the first row are calculated assuming row carry-out bits of 0 and 1 from a second row of adders preceding the first row.

The examiner respectfully submits that the claims, particularly the independent claims, do not require or defined specific adder as the first adder or second adder but rather the claims define a least significant ADDER CELL thus the cited reference by Uya does not need to disclose the Bit 0 adder receive any conditional carry-out bits wherein the first set of adder in Figure 2 can be considered as the least significant ADDER CELL. Second, the conditional carry-out bit is generated based on the ASSUMPTION or ACKNOWLEGDEMENT of value of the carry-in bit which is expressively seen in the Figure 2, thus the term "CONDITIONAL".

c. The applicant argues in pages 18-19 for claims rejected under 35 U.S.C. 102(b) that the cited reference by Uya fails to disclose the step of propagating the received conditional carryout bits through a first pass gate and a second pass gate respectively when the first input data bit and the second input data bit are unequal.

The examiner respectfully submits that the cited reference by Uya clearly and expressively discloses the above argued limitation. First, the claims do not define or address specifically what are the first and second pass gate respectively. Thus, as long as the cited reference discloses conditional carry-out bits are passing through logic gates, it would meet the claimed invention. The examiner would like to point out Figure 2 of the cited reference clearly teaches the above argued limitations, particularly (as an example) logic gate XOR and logic NAND 34, wherein NAND gate would pass first conditional carry-out bit $C_{x+1}1$ and the

corresponding XOR gate would pass the second conditional carry-out bit $C_{x+1}0$ whenever Ax and Bx are opposite, these conditional carry-out bits $C_{x+1}1 == 1$ and $C_{x+1}0 == 0$ as seen in Figures 3-4. These values 1 and 0 are high values for $C_{x+1}1$ and $C_{x+1}0$ respectively to propagate up to the next adder in-line.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

February 20, 2008

/Chat C. Do/
Primary Examiner, Art Unit 2193

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	09/667,164	BALLACHINO, WILLIAM E.	
	Examiner	Art Unit	
	CHAT C. DO	2193	